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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,399	04/14/2005	Franciscus Johannes Klosters	NL02 1019 US	8141

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EXAMINER	
FONG, VINCENT	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,399	KLOSTERS ET AL.	
	Examiner	Art Unit	
	Vincent Fong	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4-14-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 04-14-2005.

Claims 1-9 are pending and have been examined.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed 04-14-2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the publication date (12-19-2000) and name of applicant (Hongbin Hao Jerry) does not match with the document code (1163586) for cite number 1. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Objections

3. Claim 1,2,4,6,7 and 9 are objected to because of the following informalities:

As per claim 1, the meaning of the terms "ones of the bits" (line 4,8,11) and "ones of the series" (line 11,12) is unclear, they should be changed to "ones of the temporally successive bits" and " ones of the series of instructions" and will be treat as such in the examination.

As per claim 2, the meaning of the term "ones of the bits" (line 5) is unclear, it should be changed to "ones of the temporally successive bits" and will be treat as such in the examination.

As per claim 4, the meaning of the term "the instructions" (line 3) is unclear; it should be changed to "the instruction in the series" and will be treat as such in the examination.

As per claim 6, the term "the bits that contribute to the data word"(line 3) lack antecedent basis, it should be changed to "bits that contribute to the data word" and will be treat as such in the examination.

As per claim 7, the terms "the presence"(line 2), "the bits that contribute to the data word"(line 3) and "the trigger signal"(line 3) lack antecedent basis, it should be changed to "presence", "bits that contribute to the data word" and "execution trigger signal" and will be treat as such in the examination.

As per claim 9, the term "one of the bits" (line 5,9), "the instructions" (line 6) and "one of the series" (line 8,9) lack antecedent basis, it should be changed to "one of the temporally successive bits", "the series of instructions" and "one of the series of instructions" and will be treat as such in the examination.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the phrase "and or" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. If applicant's intent to claim "and/or", please note that the broadest reasonably interpretation of that claim language would be "or". The limitation is treated as "and" for the examination.

Any claim not specifically addressed above, is being rejected as incorporating the deficiencies of a claim upon which it depends.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,2,4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hongbin Hao et al. (USPN 6163586, hereinafter Hao).

As per claim 1, Hao discloses:

A data processing apparatus (element 10 figure 4), the apparatus comprising: an input port (element 14 figure 4) for receiving a communication signal that contains temporally successive bits [figure 3 display the temporally successive bits received by the input port (column 3 lines 38-41)]; an output port (element 16 figure 4) for outputting a data word formed from respective ones of the temporally successive bits [figure 3 display the echo of the received data word which is sent out through output port (column 3 lines 38-41)]; a programmable processor circuit (element 12 figure 4) coupled to the input port, the processor executing a plurality of series of programmed instructions in support of said receiving and outputting [figure 5 show the operation the processor carry out in support of receiving; by setting the character configuration of the incoming stream, and outputting by setting the echoing (abstract)] , each at a time of reception of a respective ones of the temporally successive bits , the processor circuit suspending operation each time after executing a respective one of the series of instructions [figure 5 shows that at step 62 after receiving the previous bit, the processor is suspend wait for the new start bit (next bit in the data word) is received (column8 line 24-28)]; a synchronization circuit (element 32, 20 figure 4) coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective ones of the temporally successive bits [the synchronization circuit receives the signal coming into the input port (column 6 lines 62-66) and the circuit triggers

different flow of operation depending the bit it received (column 7 line 60 to column 8 line 17)], and, except for a last one of the series, prior to reception of one or more later bits that contribute to the data word [the operation are trigger by the received data bit by bit (column 7 line 60 to column 8 line 17)].

As per claim 2, the rejection of claim 1 is incorporated and Hao further discloses: the programmable processor (element 12 figure 4) is programmed to compute cumulative information [the state in the flow diagram of figure 5], corresponding to a function of a combination of the bits from which the data word is formed [the determination of the character received from the received bits (column 7 line 60 to column 8 line 17)], each series of instructions being programmed to add a contribution (the new state in the flow of figure 5) to the cumulative information (the old state in the flow of figure 5) of the respective ones of the temporally successive bits at the time of reception of which the series is executed [the changing state in the flow depending on the series of bit received previously (column 7 line 60 to column 8 line 17)].

As per claim 4, the rejection of claim 1 is incorporated and Hao further discloses: the processor circuit is constructed sequence instruction execution [the operation executed by the circuit depends on the state of the flow in figure 5]; the operation is inherently triggered by some signals(using handshake signals), execution of each of the instruction in the series being triggered by a respective request signal [each operation is triggered by receiving a new data bit through input port (column 7 line 60 to column 8

line 17)], execution of each instruction of the series, except for a last instruction in each series, generating the request signal for a next one of the instructions in the series [each operation trigger a next step or repeat the same operation (active wait) (figure 5)], the synchronization circuit being coupled to apply the request signals for the initial one of the instructions in the series [the synchronization circuit receives the signal coming into the input port (column 6 lines 62-66) and the circuit trigger the operation in the flow].

As per claim 5, the rejection of claim 1 is incorporated and Hao further discloses: the synchronization circuit (element 32, 20 figure 4) is arranged to adapt a frequency of triggering the execution of the series of instructions under control of a timing of transitions in the communication signal [the incoming signal is analysis to determine the value of M by the baud rate determination means and the value of M is sent to the synchronization circuit (column 7 lines 13-26) through the usage of value M (BT, BT=32M column 7 lines 57-60) the synchronization circuit is adapt to the frequency to sample the data input (column 7 line 60 to column 8 line 17) thus triggering the operation in changing in flow of figure 5], since the synchronization circuit is arranged to operate as such, it is inherent that it contains an adaptable timer circuit.

As per claim 6, the rejection of claim 5 is incorporated and Hao further discloses: the synchronization circuit inherently has the adaptable timer circuit (see rejection of claim 5), and the circuit is arranged to measure a duration of a synchronization interval in the communication signal preceding bits (start bits) that contribute to the data word

[measure the duration of the start bit to determine the baud rate (column 7 line 60 to column 8 line 17)], and to set the frequency that will be used to trigger execution of the series of instructions dependent on the measured duration [the synchronization circuit is adapt to the frequency to sample the data input (column 7 line 60 to column 8 line 17) thus triggering the operation in changing in flow of figure 5].

As per claim 7, the rejection of claim 6 is incorporated and Hao further discloses: the timer circuit is arranged to detect presence or absence of a validation part (start bits) in the communication signal prior to bits that contribute to the data word (start bit is not part of the character received), the timer circuit generating trigger signals only upon detection of the presence of the validation part [timer circuit would not calculate value of M and BT till the detection of start bits thus would not enable the synchronization circuit to further trigger operation in the flow of figure 5 (column 7 lines 47-64)].

As per claim 8, the rejection of claim 1 is incorporated and Hao further discloses: the processor circuit (element 12 figure 4, The operand length, is not patentably distinct as it is possible that the operand length of the instruction executed by the processor in the prior art could be changed and there would be no difference in performance over the processor of the prior art. See MPEP 2144.04 section IV).

As per claim 9, see the similar rejection of claim 1.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hao in view of Wishneusky et al. (USPN 4975828, hereinafter Wishneusky).

As per claim 3, the rejection of claim 2 is incorporated and Hao discloses the limitations in claim 2.

Hao does not disclose the cumulative information comprises one or more parity bits. However, Wishneusky discloses a data processing apparatus (figure 2) that support the calculation of parity in a cumulative bit by bit fashion (column 27 lines 21-25, column 29 lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the cumulative calculation parity instruction into the series to series of instructions to calculate parity as part of the cumulative information in the apparatus

of Hao because Wishneusky teaches that inclusion of such instruction can help the apparatus performance in time critical task associated with receiving and sending of data word (Wishneusky column 6 lines 28-32). Including the cumulative calculation of parity further enhances the speed of the method of baud rate detection and character configuration in Hao by speeding up the process of assembling the incoming predetermined characters (AT or at) (Hao column 1 lines 59-64).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nguyen et al. (USPN 6167466) discloses a data processing device, which adjust the speed of it operation according to the speed of the incoming signals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on 7:00-3:30 Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Fong
March 12, 2007 VF

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